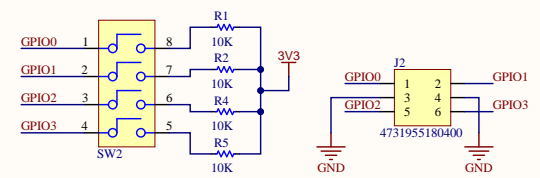
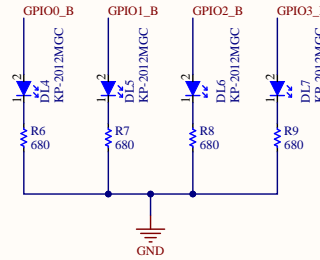
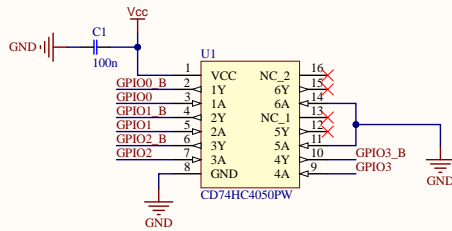
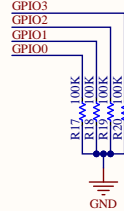
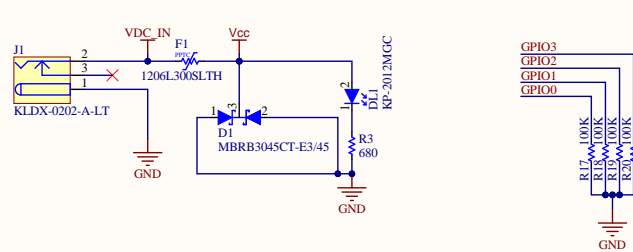


A

A

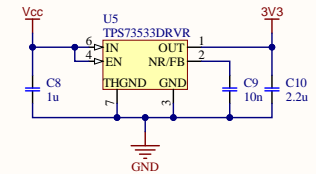
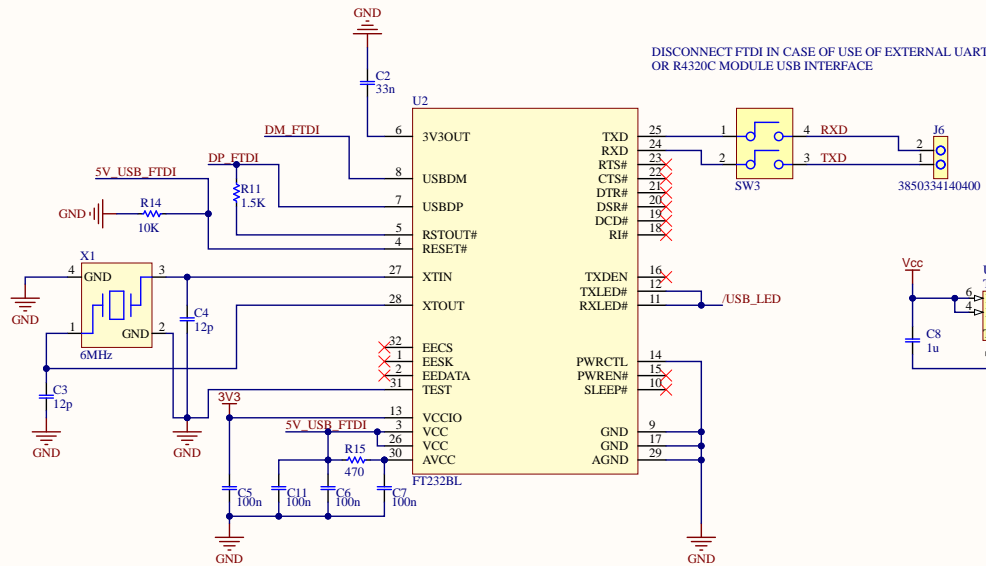
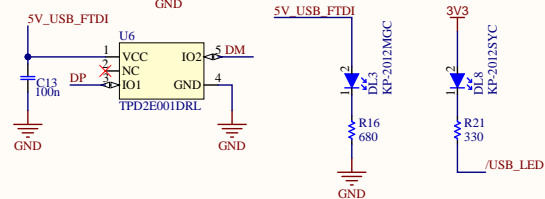
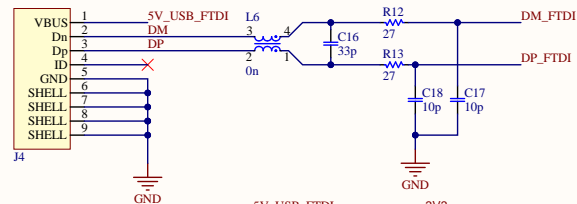
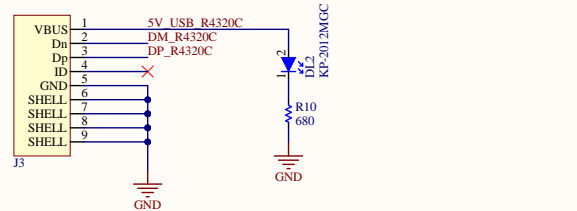


SW open to be used when:
- GPIO is configured as OUT
- GPIO is configured as IN and forced at LOW level
- GPIO is configured as IN and driven externally through J2

SW closed to be used when:
- GPIO is configured as IN and forced at HIGH level

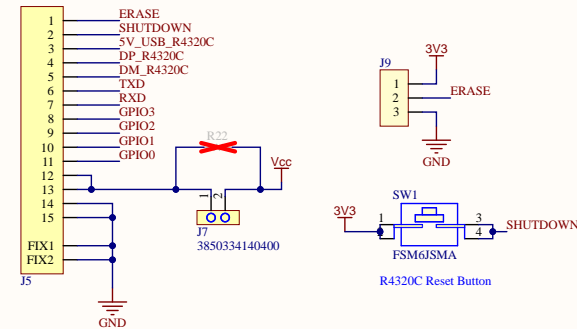
B

B



C

C



D

D

RESERVED DOCUMENT



Model : Mod. R4320CEVB

Sheet Description: TOP

Pcb Code: BR43202047EV

Filename and full path: R4320CEVB_Top.SchDoc

Date: 24/11/2020 10:35:23

Sheet 1 of 1

Revision
PCB/SCH
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